A DATA TRANSFERRING APPARATUS FOR TRANSFERRING LIQUID EJECTION DATA AND A LIQUID EJECTING APPARATUS

BACKGROUND OF THE INVENTION

[0001] This application claims priority from a Japanese Patent Application No. 2003-190388 filed on July 2, 2003, the content of which is incorporated herein by reference.

Field of the Invention

[0002] The present invention relates to a data transferring apparatus for transferring liquid ejection data and a liquid ejecting apparatus of liquid ejection data for transferring the liquid ejection data to a liquid ejecting head, wherein the liquid ejection data is inputted into the liquid ejecting apparatus which ejects a liquid such as ink from the liquid ejecting head onto a medium to be ejected.

Description of the Related Art

[0003] A liquid ejecting apparatus called an inkjet type recording apparatus records image data by ejecting ink from a recording head onto recording papers. The inkjet type recording apparatus ejects ink droplets of plural colors from plural nozzle arrays, which are provided at the head face of the recording head, developing image data, which has been compressed to be capable of line development, to bitmap images in line and forming the developed bitmap images on the recording side of the recording papers. It forms images on the recording papers by ejecting ink droplets of plural colors to form plural ink dots. Further, the compressed data capable of the line development is, for example, the compressed data by the run length compression method, which is generally widely known, capable of sequentially developing data per byte unit.

[0004] This inkjet type recording apparatus generally has a data transferring apparatus for receiving image data compressed to be capable of the line development inputted from an external apparatus such as a personal computer, developing (extracting) the inputted compressed data in line, performing data processes required for the developed bitmap images and then transferring the data to a register of the recording head. The generally conventional data transferring apparatus is configured, for example, as shown in Fig. 15.

[0005] The data transferring apparatus 10 has a system bus SB as a data transfer route. To the system bus SB, a microprocessor (MPU) 11, a RAM 12 and a head controlling unit 13 are coupled so as to transfer data, and a recording head 62 is coupled to the head controlling unit 13. The compressed recording data transferred from an information processing apparatus such as a personal computer or a digital camera, which is not shown in the drawing, is stored in the RAM 12 via the system bus SB.

[0006] The compressed recording data stored in a compressed data storing area of the RAM 12 is sequentially transferred to the microprocessor 11 via the system bus SB one byte each (a route represented by the symbol A), sequentially extracted by a program in accordance with an extraction sequence one byte each, then transferred to the RAM 12 via the system bus SB one byte each once more (a route represented by the symbol B) and then stored a desired bitmap image area of the RAM 12. When the developed data has been completely stored in the bitmap image area of the RAM 12, the developed data in the bitmap image area of the RAM 12 is transferred to a register (not shown in the drawing) in the head controlling unit 13 via the system bus SB one byte each (a route represented by the symbol C) and ink is ejected from each of the nozzle arrays of the recording head 62 onto the recording papers based on these bitmap images.

[0007] In addition, as an example of the prior art to speed

up the data transfer process, it is well-known that two independent buses, a system bus and a local bus, are provided and two bus controllers are provided between the system bus and the local bus. In regard to the data transferring apparatus, parallel processing is performed, that is, one bus controller accesses a main memory which is coupled to the system bus while the other bus controller accesses the local memory which is coupled to the local bus so that the data transfer process can speed up as disclosed, for example, Japanese Patent Publication No. 3251053.

[0008] To enhance the performance speed of liquid ejection in regard to the data transferring apparatus 10 of the conventional liquid ejecting apparatus configured as shown in Fig. 15, in other words, to further increase the recording speed in regard to the inkjet type recording apparatus, there are some obstacles as mentioned below.

[0009] First, since the compressed recording data is developed (extracted) by a program one byte each, it is impossible to process a great quantity of compressed data at high speed. If the microprocessor 11, which operates at high speed clock and has a high process capacity, is used, speeding up can be achieved, however, that causes such problem as the cost of the data transferring apparatus 10 gets extremely high if this expensive microprocessor 11 is mounted.

[0010] In addition, since both the data transfer to the RAM 12 and the data transfer from the RAM 12 are performed through the microprocessor 11, while the microprocessor 11 executes other data processes or calculations such as the microprocessor 11 fetches programs from the RAM 12, the data transfer might get into a waiting state, and thus the data transfer delay occurs, so that the data transfer at high speed can not be achieved.

[0011] Further, since the same route is used for both the access route from the microprocessor 11 to the RAM 12 via the system bus SB and the data transfer route from the Ram 12 to the recording

head 62, the system bus SB is occupied while the microprocessor 11 accesses the RAM12, so that the data transfer from the RAM 12 to the recording head 62 cannot be performed during that time. For this reason, the data transfer delay to the recording head 62 occurs, and thus the data transfer rate cannot speed up.

[0012] Further, in regard to the prior art disclosed in the Japanese Patent Application Publication No. 3251053 described above, the compressed recording data is also developed (extracted) by a program one byte each, so that a great amount of compressed data cannot be developed at high speed. Therefore, in regard to the liquid ejecting apparatus such as the recording apparatus, which executes recording by developing the compressed recording data transferred from an information processing apparatus and then transferring it to the recording head, the speed of ejecting liquid cannot be enhanced because the process to develop the compressed data is still slow though the data transfer process can be performed at high speed.

SUMMARY OF THE INVENTION

[0013] It is an object of the present invention to realize the development process of compressed data at high speed and the data transfer to the liquid ejecting head at high speed at low cost, so that it is possible to considerably increase the liquid ejection speed of the liquid ejecting apparatus at low cost compared with that of the prior art.

[0014] To achieve the object above, according to the first aspect of the present invention, a data transferring apparatus for transferring liquid ejection data, comprises a system bus,

a system memory coupled to the system bus in order to be able to transfer data to the system bus and a decode unit comprising a decode circuit coupled to the system bus in order to be able to transfer data to the system bus, wherein the decode circuit

can perform hardware development on liquid ejection data compressed to be capable of line development, and a data transferring unit for transferring the liquid ejection data compressed to be capable of line development to the decode circuit via the system bus and transferring the developed liquid ejection data to the system bus.

[0015] In this way, the decode circuit performs hardware development on the compressed liquid ejection data, which used to be developed by a conventional program. That is, by independently performing only the development of the compressed data by the decode circuit, which is exclusively used for developing compressed data, rather than developing the compressed data by a program of single thread, which sequentially performs various data processes besides the development process of the compressed data, it is possible to perform the development process of the compressed recording data at high speed.

[0016] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the first aspect of the present invention, since it is possible to realize the development process of compressed data at high speed and the data transfer to the liquid ejecting head at high speed at low cost by the decode unit comprising the decode circuit coupled to the system bus in order to transfer data, the action and effect that it is possible to considerably increase the liquid ejection speed of the liquid ejecting apparatus at low cost compared with that of the prior art can be obtained.

[0017] According to the second aspect of the present invention, in regard to the first aspect described above, the decode unit further comprises a line buffer for storing the liquid ejection data developed by the decode circuit by word unit, and a DMA transferring unit for performing DMA transfer on the liquid ejection data compressed to be capable of line development to the decode circuit from the system memory, performing DMA transfer on the liquid ejection data developed in the line buffer to the

system memory by word unit, and performing sequential DMA transfer on the developed liquid ejection data stored in the system memory to a register of a liquid ejecting head.

[0018] In this way, since the line buffer is provided to store the developed data per word unit, the compressed data developed by a conventional program one byte each is developed per word unit (2 bytes), stored in the line buffer and transferred per word unit. That is, since the amount of the compressed data to be transferred at a time becomes twice that of the conventional way, the development process of the compressed data can be performed at high speed. Further, the high-speed data transfer can be achieved by the DMA (Direct Memory Access) transfer. The DMA transfer is such well-known transfer method as once addresses of a transfer source and a transfer destination or the number of transfer are set in a register, then the data transfer can be performed at high speed by hardware without a microprocessor.

[0019] According to the third aspect of the present invention, in regard to the second aspect described above, the line buffer further comprises two (2) faces of buffer areas for storing developed data of predetermined words, the liquid ejection data developed by the decode circuit is sequentially stored in a first face of the buffer areas, while the liquid ejection data developed by the decode circuit is sequentially stored in a second face of the buffer areas when the developed data of predetermined words is accumulated, and DMA transfer to the system memory is performed per predetermined words with respect to the developed data when the developed data of predetermined words is accumulated.

[0020] In this way, the line buffer has two faces of buffer areas which are capable of storing the developed data of predetermined bytes, and stores the data which has been developed by the decode circuit in a first face of the buffer areas, and when predetermined bytes have been accumulated, the developed data of the first face is transferred per word unit by the DMA transferring

means, while the data developed by the decoded circuit can be stored in a second face of the buffer areas, so that it is possible to perform development process of compressed recording data and data transfer process in parallel.

[0021] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the third aspect of the present invention, added to the second aspect described above, the development process of compressed recording data and the data transfer process can be perform in parallel, and thus the action and effect that it is possible to further increase the liquid ejection speed of the liquid ejecting apparatus can be obtained.

[0022] According to the fourth aspect of the present invention, a data transferring apparatus for transferring liquid ejection data, comprises a system bus, an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development, a receiving buffer unit comprising an interface memory for storing liquid ejection data compressed to be capable of line development, a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development and stored in the interface memory, a system memory for storing the liquid ejection data developed in the decode circuit and a head controlling unit comprising a register of a liquid ejecting head, wherein the interface unit, the receiving buffer unit, the decode unit and the system memory are coupled to the system bus in order to be able to transfer data.

[0023] The liquid ejection controlling data including the liquid ejection data compressed to be capable of the line development, received by the interface unit, is temporarily stored into the interface memory of the receiving buffer unit via the system bus, and transferred from the receiving buffer unit to the decode unit via the system bus. And, in the decode circuit in

the decode unit, after the liquid ejection data compressed to be capable of the line development is developed, it is stored into the system memory via the system bus. In this way, the decode circuit performs hardware development on the compressed liquid ejection data on which a conventional program used to perform software development. That is, by independently performing only the development of the compressed data by the decode circuit, which is exclusively used for developing compressed data, rather than developing the compressed data by a program of single thread, which sequentially performs various data processes besides the development process of the compressed data, it is possible to perform the development process of the compressed recording data at high speed.

[0024] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the fourth aspect of the present invention, since it is possible to realize the development process of compressed data at high speed and the data transfer to the liquid ejecting head at high speed by the decode unit comprising the decode circuit coupled to the system bus in order to transfer data, the action and effect that it is possible to considerably increase the liquid ejection speed of the liquid ejecting apparatus compared with that of the prior art can be obtained.

[0025] According to the fifth aspect of the present invention, in regard to the fourth aspect described above, the decode unit further comprises a line buffer for storing the liquid ejection data developed by the decode circuit by word unit, and a DMA transferring unit for performing DMA transfer on the liquid ejection data compressed to be capable of line development to the decode circuit from the interface memory, performing DMA transfer on the liquid ejection data developed in the line buffer to the system memory by word unit, and performing sequential DMA transfer on the developed liquid ejection data stored in the system memory

to a register of a liquid ejecting head.

[0026] In this way, since the line buffer is provided to store the developed data per word unit, the compressed data developed by a conventional program one byte each is developed per word unit (2 bytes), stored in the line buffer and transferred per word unit. That is, since the amount of the compressed data to be transferred at a time becomes twice that of the conventional way, the development process of the compressed data can be performed at high speed. Further, the high-speed data transfer can be achieved by the DMA (Direct Memory Access) transfer. The DMA transfer is such well-known transfer method as once addresses of a transfer source and a transfer destination or the number of transfer are set in a register, then the data transfer can be performed at high speed by hardware without a microprocessor.

[0027] According to the sixth aspect of the present invention, in regard to the fifth aspect described above, the line buffer further comprises two (2) faces of buffer areas for storing developed data of predetermined words, the liquid ejection data developed by the decode circuit is sequentially stored in a first face of the buffer areas, while the liquid ejection data developed by the decode circuit is sequentially stored in a second face of the buffer areas when the developed data of predetermined words is accumulated, and DMA transfer to the system memory is performed per predetermined words with respect to the developed data when the developed data of predetermined words is accumulated.

[0028] In this way, the line buffer has two faces of buffer areas, which are capable of storing the developed data of predetermined bytes, and stores the data, which has been developed by the decode circuit in a first face of the buffer areas, and when predetermined bytes have been accumulated, the developed data of the first face is transferred per word unit by the DMA transferring means, while the data developed by the decoded circuit can be stored in a second face of the buffer areas, so that it is possible to

perform development process of compressed recording data and data transfer process in parallel.

[0029] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the sixth aspect of the present invention, added to the fifth aspect described above, the development process of compressed recording data and the data transfer process can be perform in parallel, and thus the action and effect that it is possible to further increase the liquid ejection speed of the liquid ejecting apparatus can be obtained.

[0030] According to the seventh aspect of the present invention, in regard to the sixth aspect described above, further comprises a first dedicated bus for coupling the interface unit to the receiving buffer unit, a second dedicated bus for coupling the receiving buffer unit to the decode unit and a third dedicated bus for coupling the decode unit to the head controlling unit, wherein the receiving buffer unit further comprises a command storing register which is accessible from the system bus, a header analyzing unit for analyzing a header of the liquid ejection controlling data, a command separating unit for separating a command from the liquid ejection controlling data according to the analysis result of the header analyzing unit and storing the command into the command storing register, and a data transfer controlling unit for storing liquid ejection controlling data, from which the command is separated, into the interface memory.

[0031] Further, in regard to the liquid ejection controlling data transferred from the interface unit to the receiving buffer unit via the first dedicated bus, its header is analyzed by the header analyzing means of the receiving buffer unit. In regard to the liquid ejection controlling data of which the header has been analyzed, the command is separated and stored in the command storing register based on this analysis result, and the liquid ejection controlling data, from which the command has been

separated, is stored in the interface memory by the data transfer controlling means. The command is the control command for performing liquid ejection control. The command stored in the command storing register is accessed by the microprocessor via the system bus, and the microprocessor analyzes the command and performs the liquid ejection control based on the command. And, the liquid ejection controlling data stored in the interface memory is transferred to the decode unit via the second dedicated bus, then the liquid ejection data, which is included in the liquid ejection controlling data, compressed to be capable of the line development is developed by the decode unit, then it is stored in the system memory via the system bus in advance, and then it is transferred from the decode unit to the register of the head controlling unit via the third dedicated bus. That is, the header analysis process of the liquid ejection controlling data, on which a conventional program performs software process, and the processes of storing the command into the command storing register and storing the compressed recording data into the interface memory by separating the command from the liquid ejection controlling data based on the header analysis result are performed in the receiving buffer unit. And, the liquid ejection controlling data received by the interface unit is transferred to the receiving buffer unit via the first dedicated bus, the liquid ejection controlling data stored in the interface memory of the receiving buffer unit is transferred to the decode unit via the second dedicated bus, the liquid ejection data compressed to be capable of the line development, included in the liquid ejection controlling data, is developed by the decode circuit and the developed liquid ejection data is transferred to the head controlling unit via the third dedicated bus. Owing to this, since the data transfer load of the system bus and the processing load of the microprocessor on the system bus can be significantly reduced, the data transfer, wherein the dependence on the microprocessor is considerably low,

can be achieved and the data transfer processes between the interface unit and the decode unit and between the decode unit and the liquid ejecting head can be performed at higher speed.

[0032] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the seventh aspect of the present invention, added to the sixth aspect described above, since the data transfer load of the system bus and the processing load of the microprocessor on the system bus can be significantly reduced, besides the data transfer processes between the interface unit and the decode unit and between the decode unit and the liquid ejecting head can be performed at higher speed, the action and effect that it is possible to further increase the liquid ejection speed of the liquid ejecting apparatus can be obtained.

[0033] According to the eighth aspect of the present invention, in regard to the sixth aspect described above, further comprises a first dedicated bus for coupling the interface unit to the receiving buffer unit, a second dedicated bus for coupling the receiving buffer unit to the decode unit and a third dedicated bus for coupling the decode unit to the head controlling unit, wherein the interface unit comprises a command storing register which is accessible from the system bus, a header analyzing unit for analyzing a header of the liquid ejection controlling data, a command separating unit for separating a command from the liquid ejection controlling data according to the analysis result of the header analyzing unit and storing the command into the command storing register, and a data transfer controlling unit for storing liquid ejection controlling data, from which the command is separated, into the interface memory.

[0034] In regard to the liquid ejection controlling data received by the interface unit, its header is analyzed by the header analyzing means of the interface unit. In regard to the liquid ejection controlling data of which the header has been analyzed,

the command is separated and stored in the command storing register based on this analysis result, and the liquid ejection controlling data, from which the command has been separated, is stored in the interface memory of the receiving buffer unit by the data controlling means via the first dedicated bus. The command stored in the command storing register is accessed by the microprocessor via the system bus, and the microprocessor performs the command analysis. And, the liquid ejection controlling data stored in the interface memory is transferred to the decode unit via the second dedicated bus, then the liquid ejection data, which is included in the liquid ejection controlling data, compressed to be capable of line development is developed by the decode unit, then it is stored in the interface memory via the system bus in advance, and then it is transferred to the register of the head controlling unit via the third dedicated bus from the decode unit. That is, the header analysis process of the liquid ejection controlling data, on which a conventional program performs software process, and the processes of storing the command into the command storing register and storing the compressed recording data into the interface memory by separating the command from the liquid ejection controlling data based on the header analysis result are performed in the interface unit. And, the liquid ejection controlling data, from which the command is separated by the command analysis of the interface unit, is transferred to the receiving buffer unit via the first dedicated bus and stored in the interface memory, the liquid ejection controlling data stored in the interface memory of the receiving buffer unit is transferred to the decode unit via the second dedicated bus, the liquid ejection data developed by the decode circuit, is transferred to the head controlling unit via the third dedicated bus. Owing to this, the data transfer load of the system bus and the processing load of the microprocessor on the system bus can be significantly reduced, and besides the data transfer processes between the interface unit

and the decode unit and between the decode unit and the liquid ejecting head can be performed at higher speed.

[0035] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the eighth aspect of the present invention, added to the sixth aspect described above, since the data transfer load of the system bus and the processing load of the microprocessor on the system bus can be significantly reduced, besides the data transfer processes between the interface unit and the decode unit and between the decode unit and the liquid ejecting head can be performed at higher speed, the action and effect that it is possible to further increase the liquid ejection speed of the liquid ejecting apparatus can be obtained.

[0036] According to the ninth aspect of the present invention, in regard to the seventh or eighth aspects described above, the receiving buffer unit further comprises a data separating unit for separating the liquid ejection controlling data stored in the interface memory into a remote command and liquid ejection data compressed to be capable of line development, the remote command is processed by a microprocessor coupled to the system bus, and the liquid ejection data compressed to be capable of line development is transferred to the decode unit.

[0037] Here, the remote command is a command, wherein any header is not attached, such control command as interruption control or reset control during liquid ejection control execution by the command. In case the liquid ejection controlling data, wherein this remote command is stored in the interface memory also includes the liquid ejection data compressed to be capable of line development, since the data separating means for separating the remote command and the liquid ejection data compressed to be capable of line development is provided in the receiving buffer unit in order that the microprocessor processes only the remote command via the system bus, only the liquid ejection data compressed to

be capable of line development can be transferred to the decode unit.

[0038] According to the tenth aspect of the present invention, in regard to the fourth aspect described above, further comprises a first dedicated bus for coupling the interface unit to the receiving buffer unit, a second dedicated bus for coupling the receiving buffer unit to the decode unit and a third dedicated bus for coupling the decode unit to the head controlling unit, wherein the receiving buffer unit further comprises a data transfer controlling unit for storing liquid ejection controlling data received by the interface unit into the interface memory, and a data separating unit for separating the liquid ejection controlling data stored in the interface memory into a command and liquid ejection data compressed to be capable of line development, wherein the command is processed by a microprocessor coupled to the system bus, and the liquid ejection data compressed to be capable of line development is transferred to the decode unit.

[0039] The liquid ejection controlling data transferred from the interface unit to the receiving buffer unit via the first dedicated bus is stored in the interface memory. The liquid ejection controlling data is stored in the interface memory is separated into the command and the liquid ejection data compressed to be capable of line development by the data separating means when it is transferred to the decode unit via the second dedicated bus. The command is a controlling command for performing the liquid ejection control. The command is processed by the microprocessor via the system bus, and the microprocessor analyzes the command to perform the liquid ejection control based on the command. And, the liquid ejection data compressed to be capable of line development is transferred to the decode unit via the second dedicated bus, then developed by the decode circuit, and then transferred to the register of the head controlling unit via the third dedicated bus after stored in the system memory via the system

bus in advance. Further, the command includes, for example, a remote command which is such control command as interruption control or reset control during liquid ejection control execution.

[0040] That is, when the liquid ejection controlling data received by the interface unit is transferred to the receiving buffer unit via the first dedicated bus, and the liquid ejection controlling data stored in the interface memory of the receiving buffer unit is transferred to the decode unit via the second dedicated bus, the process separating the command and the remote command from the liquid ejection controlling data on which a conventional program performs software process are performed in the receiving buffer unit. And, the liquid ejection data compressed to be capable to line development is developed by the decode circuit, and the developed liquid ejection data is transferred to the head controlling unit via the third dedicated bus. Owing to this, since the data transfer load of the system bus and the processing load of the microprocessor on the system bus can be significantly reduced, data transfer can be performed while the dependence on the microprocessor is considerably low, and thus the data transfer processes between the interface unit and the decode unit and between the decode unit and the liquid ejecting head can be performed at higher speed.

[0041] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the tenth aspect of the present invention, added to the fourth aspect described above, since the data transfer load of the system bus and the processing load of the microprocessor on the system bus can be significantly reduced, besides the data transfer processes between the interface unit and the decode unit and between the decode unit and the liquid ejecting head can be performed at higher speed, the action and effect that it is possible to further increase the liquid ejection speed of the liquid ejecting apparatus can be obtained.

[0042] According to the eleventh aspect of the present invention, in regard to the fourth aspect described above, one (1) ASIC comprises the interface unit, the receiving buffer unit, the decode unit, the head controlling unit and the first, second and third dedicated buses.

[0043] In this way, since the interface unit, the receiving buffer unit, the decode unit and the head controlling unit are configured as circuit blocks in the same ASIC, and the first, second and third dedicated buses, which couple them respectively, is configured to be in the same ASIC, high speed DMA transfer can be performed particularly with one clock. Therefore, the compressed liquid ejection data can be transferred to the decode unit at higher speed.

[0044] Owing to this, according to the data transferring apparatus for transferring liquid ejection data relating to the eleventh aspect of the present invention, added to the fourth aspect described above, since the compressed liquid ejection data can be transferred to the decode unit at higher speed, and besides the transfer of the developed liquid ejection data to the liquid ejecting head from the system memory can be performed at high speed, the action and effect that it is possible to further increase the liquid ejection speed of the liquid ejecting apparatus can be obtained.

[0045] According to the twelfth aspect of the present invention, in regard to the first aspect described above, the compressed liquid ejection data is run length compression data, and the decode circuit can perform hardware development on run length compression data.

[0046] According to the data transferring apparatus for transferring liquid ejection data relating to the twelfth aspect of the present invention, by the decode circuit whereby the run length compressed data capable of line development can be hardware-developed, the action and effect in the first aspect

described above can be achieved.

[0047] According to the thirteenth aspect of the present invention, a liquid ejecting apparatus comprises a data transferring apparatus by one of the first to twelfth aspects described above.

[0048] According to the liquid ejecting apparatus relating to the thirteenth aspect of the present invention, in regard to the liquid ejecting apparatus, the action and effect by one of the first to twelfth aspects described above can be obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

[0049] The above and other objects, features and advantages of the present invention will become more apparent from the following description of the presently preferred exemplary embodiments of the invention taken in conjunction with the accompanying drawings, in which:

[0050] Fig. 1 is a plan view of an inkjet type recording apparatus relating to the present invention.

[0051] Fig. 2 is a side view of an inkjet type recording apparatus relating to the present invention.

[0052] Fig. 3 is a block diagram of an inkjet type recording apparatus relating to the present invention.

[0053] Fig. 4 is a block diagram showing the configuration of a data transferring apparatus.

[0054] Fig. 5 is a timing chart schematically showing the flow of data.

[0055] Fig. 6 is a block diagram showing the configurations of the DECU and the receiving buffer unit.

[0056] Fig. 7 is a diagram showing such flow as compressed recording data is developed.

[0057] Fig. 8 is a diagram showing such flow as compressed recording data is developed.

[0058] Figs. 9A to 9D are diagrams showing the recording data after development.

[0059] Fig. 10 is a block diagram showing the configuration of a data transferring apparatus.

[0060] Fig. 11 is a timing chart schematically showing the flow of data.

[0061] Fig. 12 is a block diagram showing the configurations of the DECU and the receiving buffer unit.

[0062] Fig. 13 is a block diagram showing the configuration of the header analyzing block.

[0063] Fig. 14 is a block diagram showing the configuration of the interface unit.

[0064] Fig. 15 is a block diagram showing a data transferring apparatus in regard to the prior art.

DETAILED DESCRIPTION OF THE INVENTION

[0065] Hereinafter, the preferred embodiments of the present invention will now be described based on drawings.

[0066] To begin with, a first embodiment of the inkjet type recording apparatus will be described as a "liquid ejecting apparatus" relating to the present invention. Fig. 1 is a schematic plan view of an inkjet type recording apparatus relating to the present invention, and Fig. 2 is a side view of it.

[0067] In the inkjet type recording apparatus 50, a carriage 61 is provided to move along a main scanning direction X as a recording means, which performs recording on recording papers P, rotatably supported by carriage guide shaft 51. On the carriage 61, a recording head 62 is mounted as a "liquid ejecting head", which performs recording by ejecting ink onto the recording papers P. Opposite to the recording head 62, a platen 52 is provided to control a gap between the head surface of the recording head 62 and the recording papers P. And, recording on the recording

papers P is performed by repeating an operation of transferring the recording papers P between the carriage 61 and the platen 52 in a sub scanning direction Y a predetermined amount each and an operation of ejecting ink onto the recording papers P from the recording head 62, while the recording head 62 moves back and forth once in the main scanning direction X.

[0068] A paper feeding tray 57 is configured to be capable of feeding the recording papers P such as normal papers or photo papers, and an ASF (Auto Sheet Feeder) is provided in it as a paper feeding means to automatically feed the recording papers P. The ASF is an automatic paper feeding mechanism, which has two paper feeding rollers 57b provided in the paper feeding tray 57 and a separating pad not shown in the drawing. One of these two paper feeding rollers 57b is arranged at the one side of the paper feeding tray 57, while the other one of the paper feeding rollers 57b is installed at a recording paper guide 57a, and the recording paper guide 57a is provided at the paper feeding tray 57 to be capable of sliding in the longitudinal direction corresponding to the width of the recording papers P. And, by the rotation drive force of the paper feeding roller 57b and the frictional resistance of the separating pad, the plural recording papers P stacked in the paper feeding tray 57 are automatically and accurately fed not all but a piece each during feeding.

[0069] As a recording paper carrying means for transferring the recording papers P in the sub scanning direction Y, a driving transfer roller 53 and driven transfer rollers 54 are provided. The driving transfer roller 53 is rotatably controlled by the rotation drive force such as a stepping motor, and by the rotation of the driving transfer roller 53 the recording papers P are transferred in the sub scanning direction Y. The driven transfer rollers 54 are provided as plural pieces, and each of them is urged by the driving transfer roller 53 to rotate in contact with the recording papers P, following the carriage of the recording papers

P, when the recording papers P are transferred by the rotation of the driving transfer roller 53. On the surface of the driving transfer roller 53, a film, which has high frictional resistance, is provided. By the driven transfer rollers 54, the recording papers P pressed onto the surface of the driving transfer roller 53 are firmly in contact with the surface of the driving transfer roller 53, so that they are transferred in the sub scanning direction Y by the rotation of the driving transfer roller 53.

[0070] And, a paper detector 63 is provided between the paper feeding roller 57b and the driving transfer roller 53 in the well-known art. The paper detector 63 has a lever, to which a self-resetting characteristic into an upright position is granted, pivotally supported to be rotatable only in the recording paper carriage direction, projecting toward the transfer route of the recording papers P, and is configured as the end of the lever is pushed toward the recording papers P and thus the lever is rotated, so that the recording papers P are detected. The paper detector 63 detects the starting end position and the terminal end position of the recording papers P fed by the paper feeding roller 57b, and determines a recording area corresponding to the detected positions to perform recording.

[0071] Meanwhile, a driving paper discharge roller 55 and driven paper discharge rollers 56 are provided as a means for discharging the recording papers P which have been recorded. The driving paper discharge roller 55 is rotatably controlled by the rotation drive force such as a stepping motor, and by the rotation of the driving paper discharge roller 55 the recording papers P are transferred in the sub scanning direction Y. The driven paper discharge rollers 56 have plural teeth on their circumference, and become a toothed roller, in which the end of each tooth is sharp in an acute angle, to be in contact with the recording surface of a recording paper P at point. Each of the plural driven paper discharge rollers 56 is urged by the driving paper discharge roller

55 to rotate in contact with the recording papers P, following the discharge of the recording papers P, when the recording papers P are transferred by the rotation of the driving paper discharge roller 55.

[0072] And, the rotation driving motor not shown in the drawing, which rotatably drives the paper feeding roller 57b or the driving transfer roller 53 and the driving paper discharge roller 55 and the carriage driving motor not shown the drawing, which drives the carriage 61 in the main scanning direction, are controlled by the recording controlling unit 100. In addition, the recording head is also controlled by the recording controlling unit 100 to eject ink onto the surface of the recording papers P.

[0073] Fig. 3 is a schematic flowchart of the inkjet type recording apparatus 50 relating to the present invention.

[0074] The inkjet type recording apparatus 50 has a recording controlling unit 100 for controlling various recording processes. The recording controlling unit 100 has a system bus SB. To the system bus SB, a MPU (microprocessor) 24, a ROM 21, a RAM 22 as a "system memory", a nonvolatile storage medium 23, an I/O 25 and a DECU 41 as a " decode unit" having a decode circuit 28 are coupled so as to be capable of transferring data. In the MPU 24, various calculation processes are performed. In the ROM 21, software or a program and data needed for calculation processes of the MPU 24 are stored beforehand. The RAM 22 is used as a temporarily storing area for the software or program or a working area for the MPU 24. And, in the nonvolatile storage medium 23 such as a flash memory, some data resulting from the calculation processes of the MPU 24 is stored, and it is designed to hold the data even if the power of the inkjet type recording apparatus 50 is turned off.

[0075] Further, the recording controlling unit 100 is configured to be coupled to an information processing apparatus 200 such as a personal computer via an interface unit 27, which

has an interface function with external apparatuses, and to be capable of processing input and output of various kinds of information or data with the information processing apparatus 200. And, the I/O 25 performs output control to a various motors controlling unit 31 via an input and/or output unit 26 based on the calculation process result of the MPU 24, and allows input information to be inputted from various sensors 32. The various motors controlling unit 31 is a drive control circuit, which controls various motors of the inkjet type recording apparatus 50, and is controlled by the recording controlling unit 100. And, the various sensors 32 detect various kinds of condition information of the inkjet type recording apparatus 50 and output them to the I/O 25 via the input and/or output unit 26.

[0076] During performing recording, the information processing apparatus 200 plays a host part to output record controlling data (liquid ejection controlling data) including recording data compressed by the information processing apparatus 200 in order to be capable of line development (hereinafter, referred to as compressed recording data), and the inkjet type recording apparatus 50 receives the record controlling data from the interface unit 27. The DECU 41 develops the compressed recording data with the decode circuit 28 and then stores the developed recording data in a line buffer 281. The developed recording data stored in the line buffer 281 is stored in the RAM through the system bus SB for each data of predetermined words in advance and then transferred from a register in a head controlling unit 33 to the recording head 62 through the system bus SB again via the DECU 41. The head controlling unit 33 controls the recording head 62 based on the developed recording data transferred from the RAM 22 to jet ink of various colors onto the recording papers P from the plural nozzle arrays provided on the head side of the recording head 62.

[0077] Fig. 4 is a block diagram showing the configuration

of a data transferring apparatus as a "data transferring apparatus for transferring liquid ejection data" relating to the present invention. Fig. 5 is a timing chart schematically showing the flow of recording data in a data transferring apparatus. Fig. 6 is a block diagram showing the configuration of the DECU 41.

[0078] The data transferring apparatus 10 has an ASIC (Application Specific Integrated Circuit) 4, and the ASIC 4 incorporates the interface unit 27 described above, the head controlling unit 33 described above, a receiving buffer unit 42 and a DECU 41. The DECU 41 incorporates a development processing controller 412 having the decode circuit 28 described above and the line buffer 281. And, the system bus SB is a 16 bits bus, and thus it is possible to transfer data of 1 word (2 bytes) per a predetermined data transfer period. The DECU 41 and the head controlling unit 33 are coupled by an internal bus IB in order to perform data transfer. Hereinafter, with reference to the timing chart shown in Fig. 5, the flow of data in regard to the data transferring apparatus 10 will be described.

[0079] The record controlling data sent from the information processing apparatus 200 is DMA-transferred from the interface unit 27 to the receiving buffer unit 42 via the system bus SB one word each(symbol T1). As described above, the DMA transfer is such transfer method as once addresses of a transfer source and a transfer destination or the number of transfer are set in a register then the data transfer can be performed by hardware at high speed without the MPU 24. Next, the data is DMA-transferred from the receiving buffer unit 42 to the DECU 41 via the system bus SB (symbol T2). At this time, header analysis, command analysis and remote command analysis in regard to the record controlling data are performed according a program sequence executed by the MPU 24, and only the compressed recording data is transferred to the DECU 41 one word each. Continuously, by the decode circuit 28 in the DECU 41, the compressed recording data is hardware-transferred

one word each, and the developed recording data is stored in the line buffer 281 (symbol T3).

[0080] The developed recording data stored in the line buffer 281 is DMA-transferred to the bitmap area of the RAM 22 via the system bus SB, when the recording data stored in the line buffer 281 has reached predetermined words (symbol T4). Continuously, the recording data as bitmap data stored in the bitmap area of the RAM 22 is DMA-transferred to the DECU 41 via system bus SB once again (symbol T5), then DMA-transferred from the DECU 41 to the head controlling unit 33 via the internal bus IB (symbol T6), and then DMA-transferred to the recording head 62 after stored in the register in the head controlling unit 33 (symbol T7).

[0081] Next, the DECU 41 and the receiving buffer unit 42 configured in the ASIC 4 will be described in further detail.

[0082] The DECU has, as a "DMA-transferring means", a first S-DMA controller 401, a second S-DMA controller 402, an I-DMA controller 415 and a memory controller 414 for controlling retrieving and/or writing data in regard to the RAM 22. The first S-DMA controller 401 performs DMA-transfer control between an IF memory 425 as an "interface memory" in the receiving buffer unit 42 and the development processing controller 412 via the system bus SB. The second S-DMA controller 402 performs DMA-transfer control between the development processing controller 412 and the RAM 22 via the system bus SB. The I-DMA controller 415 performs DMA-transfer control between the memory controller 414 and the head controlling unit 33 via the internal bus IB.

[0083] By the first S-DMA controller 201, the compressed recording data stored in the IF memory 425 is DMA-transferred to the development processing controller 412 one words each. The compressed recording data DMA-transferred to the development processing controller 412 is hardware-developed by the decode circuit 28 one word each, and the developed recording data is stored and accumulated in the line buffer 281. And, when the developed

recording data of predetermined words has been accumulated in the line buffer 281, the developed recording data accumulated in the line buffer 281 is DMA-transferred to the RAM 22 through the system bus SB via the memory controller 414 by the second S-DMA controller 402, and stored into the bitmap area of the RAM 22. The developed recording data stored in the bitmap area of the RAM 22 is DMA-transferred to the head controlling unit 33 through the system bus SB and the internal bus IB via the memory controller 414 by the I-DMA controller 415, and DMA-transferred to the recording head 62 after stored in the register in the head controlling unit 33.

[0084] In addition, the DMA transfer from the line buffer 281 to the RAM 22 is transferred in burst by the second S-DMA controller 402, and the DMA transfer from the RAM 22 to the recording head 62 is transferred in burst by the I-DMA controller 415. The burst transfer is such data transfer method as, when the continuous data is transferred, the data is transferred occupying a bus until all data of a predetermined data block is completely transferred by omitting a part of a sequence such as an address designation. The second DMA controller 402, when the developed recording data of predetermined bytes has been accumulated in the line buffer 281, transfers in burst the developed recording data of predetermined bytes one word each, occupying the system bus SB until the data of predetermined bytes is completely DMA-transferred to the RAM 22. The I-DMA controller 415 transfers in burst the developed recording data stored in the bitmap area of the RAM 22 one word per a data block of predetermined bytes, occupying the system bus SB until all of one data block has been completely DMA-transferred to the recording head 62. And, in case the burst transfer from the line buffer 281 to the RAM 22 and the burst transfer from the RAM 22 to the recording head 62 compete each other, the burst transfer from the RAM 22 to the recording head 62 has priority, and thus during the burst transfer from the RAM 22 to the recording

head 62 the burst transfer from the line buffer 281 to the RAM 22 is temporarily stopped, so that the ink ejecting operation from the nozzle arrays of the recording head 62 based on the recording data from the RAM 22 to the recording head 62 is not interrupted.

[0085] Fig. 7 and Fig. 8 are diagrams schematically showing the state until compressed recording data is hardware-developed in the decoded circuit 28 and stored in the line buffer 281 in the DECU 41. In addition, Fig. 9 is a diagram schematically showing the state until the developed recording data is transferred and stored from the line buffer 281 to the RAM 22.

[0086] In this embodiment, the compressed recording data has been compressed by a run length compression method. The run length compression method is a well-known data compression method and it will be briefly described below. The run length compressed data is compressed data of byte boundary, and has a set of count (1 byte) and data (1 byte or bytes). In other words, the run length compressed data is configured to first have the count and then necessarily have the data. If the value of the count is more than 128 (a negative constant), that is, more than 80H, that means repeatedly developing the next data of 1 byte, and thus the data of 1 byte following the count is repeatedly developed as many times as 257 from which the value of the count is subtracted. On the other hand, if the value of the count is less than 127, that is, less than 7FH, that means continuing data to be developed as it is without repeating after the count, and thus the data following the count is developed as it is without repetition as many times as the value of the count to which one is added.

[0087] Next, the configuration of the line buffer 281 will be described. The line buffer 281 has two faces of data storing areas of 9 words that combine storing areas of 8 words (16 bytes) and preliminary storing areas of 1 word (2 bytes), and each of faces is A face and B face respectively. The recording data developed by the decode circuit 28 one word each is sequentially

stored in one of the A face and the B face of the line buffer 281 one word each, and the data is turned to be stored into the other, face when the developed data of predetermined amount, in the present embodiment, 16 bytes has been accumulated. In addition, the accumulated data of 16 bytes, as described above, is stored in a predetermined bitmap area of the RAM 22 via the system bus SB.

[0088] In this way, the line buffer 281 has two faces of buffer areas, which are capable of storing the recording data after development of 16 bytes, and stores the recording data, which has been developed by the decode circuit 28 in a first face of the buffer areas. And, after 16 bytes have been accumulated, while the developed recording data of the first face is transferred per word unit by a DMA transferring means, the recording data developed by the decoded circuit 28 can be stored in a second face of the buffer areas, so that it is possible to perform development process of compressed recording data and data transfer process in parallel.

[0089] Continuously, as run length compressed data is taken for example, the flow of recording data will be described, wherein the compressed data is developed by the decode circuit 28, stored in the line buffer 281 and stored from the line buffer 281 to the RAM 22 (system memory).

[0090] In the IF memory 425 of the receiving buffer unit 42, the run length compressed recording data of 24 words (48 bytes), which begins from FEH as shown in the drawing, is stored. The run length compressed recording data is DMA-transferred to the decode circuit 28 via the system bus SB one word each, namely, two bytes each, hardware-developed and stored in the line buffer 281. In the present embodiment, the data starting address of the run length compressed data is an even address, and the data starting address of the bitmap data (image data) in the RAM 22 is an even address. And, the number of bytes of the data block DMA-transferred from the line buffer 281 to the RAM 22 (the number of bytes of 1 line) is 16. Further, in the IF memory 425 shown in Fig. 7,

the line buffer 281 in the DECU 41 and the system memory (RAM 22) shown in Fig. 9, the left top is an even address, and addresses become upper addresses from the left to the right in order.

[0091] Hereinafter, one word each will be described in order. First, the compressed recording data of initial 1 word (FEH, 01H) DMA-transferred from the IF memory 425 of the receiving buffer unit 42 to the decode circuit 28 in the DECU 41 (Transfer S1). The FEH is the count, and the 01H is the data. Since the value of the count of FEH is 254, that is, larger than 128, the data of 01H is repeatedly developed 257-254=3 times and 1 byte each is sequentially stored in the A face of the line buffer 281. Next, the run length compressed data DMA-transferred to the decode circuit 28 is 03H and 02H (Transfer S2). The 03H is the count, and the 02H is the data. Since the value of the count of 03H is 3, that is, smaller than 127, the data of 3+1=4 bytes following the count is developed without repetition. That is, the data of 02H, 78H, 55H and 44H following the count 03H is developed as it is without repetition, and sequentially stored in the A face of the line buffer 281 (Transfers S2 to S4). The FBH, which is the upper part (odd address part) of the DMA-transferred word data in the Transfer S4, is the count, and the next data of 1 byte is repeatedly developed 6 times (257-251=6).

[0092] Continuously, the compressed recording data DMA-transferred to the decode circuit 28 is FFH and FEH (Transfer S5). The lower address (even address) of FFH is the data, besides the data of the previous count of FBH. Therefore, FFH is repeatedly developed 6 times, and sequentially stored in the A face of the line buffer 281. And, the upper address (odd address) of FEH is the count, and the next data of 1 byte is repeatedly developed 3 times (257-254=3). Continuously, the compressed recording data DMA-transferred to the decode circuit 28 is 11H and 06H (Transfer S6). The lower address (even address) of 11H is the data, besides the data of the previous count of FEH. Therefore, 11H is repeatedly

developed 3 times, and stored in the A face of the line buffer 281. And, the upper address (odd address) of 06H is the count, and the next data (66H, 12H, 77H, 45H, 89H, 10H and 55H) of 7 bytes (6+1=7) is developed as it is without repetition, and sequentially stored in the B face of the line buffer 281 (Transfers S7 to S10).

[0093] In the mean time, when the developed recording data has been accumulated as many bytes as one line in the A face of the line buffer 281, namely, 16 bytes (at the Transfer S6), the 16 bytes are DMA-transferred to the system memory one word each as a data block of the 1 line. At that time, the second DMA controller 402 (Fig. 6) transfers data in burst, occupying the system bus SB until all the recording data after 1 line development is completely DMA-transferred to the system memory (Transfer D1). The recording data of 1 line transferred to the system memory is sequentially stored in the predetermined bitmap area of the system memory 1 word each at the first of the even address from the lower address (Fig. 9A).

[0094] Continuously, the compressed recording data DMA-transferred to the decode circuit 28 is 10H and FAH (Transfer S11). The lower address (even address) of 10H is the data, besides the data of the previous count of FBH. Therefore, 10H is repeatedly developed 6 times, and sequentially stored in the B face of the line buffer 281. And, the upper address (odd address) of FAH is the count, and the next data of 1 byte is repeatedly developed 7 times (257-250=7). Continuously, the compressed recording data DMA-transferred to the decode circuit 28 is 20H and 08H (Transfer S12). The lower address (even address) of 20H is the data, besides the data of the previous count of FAH. Therefore, 20H is repeatedly developed 7 times, and stored in the B face of the line buffer 281, and when the accumulated data in the B face has reached 16 bytes the remaining data is sequentially stored in the A face. And, the upper address (odd address) of 08H is the count, and the next data (12H, 13H, 14H, 15H, 16H, 17H, 18H, 19H and 20H) of 9

bytes (8+1=9) is developed as it is without repetition, and sequentially stored in the A face of the line buffer 281 (Transfers S13 to S17 in Fig. 8).

[0095] In the mean time, when the developed recording data has been accumulated as many bytes as 1 line in the B face of the line buffer 281, namely, 16 bytes (at the Transfer S12), the 16 bytes are DMA-transferred to the system memory one word each as a data block of the 1 line. At that time, the second DMA controller 402 (Fig. 6) transfers data in burst, occupying the system bus SB until all the recording data after 1 line development is completely DMA-transferred to the system memory (Transfer D2). The recording data of 1 line transferred to the system memory is sequentially stored in the predetermined bitmap area of the system memory 1 word each at the first of the even address from the lower address (Fig. 9B).

[0096] Continuously, the compressed recording data DMA-transferred to the decode circuit 28 is 11H and 02H (Transfer S18). The lower address (even address) of 11H is the data, besides the data of the previous count of FDH. Therefore, 11H is repeatedly developed 3 times (257-254=3), and stored in the A face of the line buffer 281, and when the accumulated data in the A face has reached 16 bytes the remaining data is sequentially stored in the B face. And, the upper address (odd address) of 02H is the count, and the next data (98H, B0H and F2H) of 3 bytes (2+1=3) is developed as it is without repetition, and sequentially stored in the B face of the line buffer 281 (Transfers S19 to S20).

[0097] In the mean time, when the developed recording data has been accumulated as many bytes as 1 line in the A face of the line buffer 281, namely, 16 bytes (at the Transfer S18), the 16 bytes are DMA-transferred to the system memory one word each as a data block of the 1 line. At that time, the second DMA controller 402 (Fig. 6) transfers data in burst, occupying the system bus SB until all the recording data after 1 line development is

completely DMA-transferred to the system memory (Transfer D3). The recording data of 1 line transferred to the system memory is sequentially stored in the predetermined bitmap area 1 word each of the system memory at the first of the even address from the lower address (Fig. 9C).

[0098] Continuously, the compressed recording data DMA-transferred to the decode circuit 28 is ABH and 03H (Transfer S21). The lower address (even address) of ABH is the data, besides the data of the previous count of FCH (the upper address of the Transfer S20). Therefore, ABH is repeatedly developed 5 times (257-252=5), and sequentially stored in the B face of the line buffer 281. And, the upper address (odd address) of 03H is the count, and the next data (FFH, FEH, FCH and FDH) of 4 bytes (3+1=4) is developed as it is without repetition, and sequentially stored in the B face of the line buffer 281 (Transfers S22 to S23).

[0099] Continuously, the compressed recording data DMA-transferred to the decode circuit 28 is FEH and FFH (Transfer S24). The lower address (even address) of FEH is the data, besides the data of the count of FEH. Therefore, FFH is repeatedly developed 3 times (257-254=3), and sequentially stored in the B face of the line buffer 281. The development processing controller 412, when the developed recording data has been accumulated as many bytes as 1 line in the B face of the line buffer 281, namely, 16 bytes (at the Transfer S24), the 16 bytes are DMA-transferred to the system memory one word each as a data block of the 1 line. At that time, the second DMA controller 402 (Fig. 6) transfers data in burst, occupying the system bus SB until all the recording data after 1 line development is completely DMA-transferred to the system memory (Transfer D4).

[0100] The recording data of 1 line transferred to the system memory is sequentially stored in the predetermined bitmap area of the system memory 1 word each at the first of the even address from the lower address (Fig. 9D). And, when the recording data

of the bitmap data for ejecting ink with one main scanning pass has been stored in the system memory, data is DMA-transferred from the system memory (RAM 22) to the internal bus IB and the head controlling unit 33. At this time, the I-DMA controller 415 (Fig. 6) transfers data in burst, occupying the system bus SB until all the recording data of the bitmap data for ejecting ink from the recording head 62 with one main scanning pass is completely DMA-transferred to the head controlling unit 33.

[0101] In this way, it is possible to perform the development process of the compressed recording data at high speed by hardware-developing the compressed recording data, which used to be software-developed by the conventional program, in the decode circuit 28. In addition, since the compressed recording data, which used to be developed one byte each by the conventional program, is developed per word unit (two bytes), it is possible to perform the development process of the compressed recording data at high speed. Therefore, since it is possible to realize the development process of the compressed data at high speed and the data transfer to the recording head 62 at high speed, it is possible to considerably increase the liquid ejection speed of the inkjet type recording apparatus 50 compared with that of the prior art.

[0102] In addition, as a second embodiment of the inkjet type recording apparatus 50 relating to the present invention, added to the first embodiment described above, dedicated buses are coupled between the interface unit 27 of the data transferring apparatus 10 and the receiving buffer unit 42 and between the receiving buffer unit 42 and the interface unit 27 respectively.

[0103] Fig. 10 is a block diagram showing the second embodiment of the data transferring apparatus 10. Fig. 11 is a timing chart schematically showing the flow of data in regard to the data transferring apparatus 10.

[0104] The interface unit 27 has a means for sending and receiving data to and from the information processing apparatus

200 taking the information processing apparatus 200 as a host apparatus in a predetermined data transfer sequence, and receives the record controlling data from the information processing apparatus 200 to allow the recording controlling unit 100 to control recording. The record controlling data includes a command and a remote command on which the MPU 24 performs command analysis and the compressed recording data on which the DECU 41 performs hardware development, and it is sent by the information processing apparatus 200 as a header of 6 bytes is added to it for each data block. The interface unit 27 DMA-transfers the received record controlling data to the receiving buffer unit 42 via a dedicated first bus IB1 at a predetermined data transfer period (symbol T11). The receiving buffer unit 42 analyzes the header of the record controlling data DMA-transferred from the interface unit 27, extracts the compressed recording data by separating the command and the remote command from the record controlling data and DMA-transfers the compressed recording data to the DECU 41 via a second dedicated bus IB2 at the next data transfer period (symbol T12).

[0105] In regard to the command included in the record controlling data, the MPU 24 accesses the receiving buffer unit 42 via the system bus SB to perform command analysis according to a program sequence executed by the MPU 24 (symbol COM). The DECU 41 develops the compressed recording data DMA-transferred from the receiving buffer unit 42 at the next data transfer period (symbol T13), and DMA-transfers it to the bitmap area of the RAM 22 via the system bus SB, when the developed recording data has been a predetermined amount (symbol T14). The recording data as the bitmap data stored in the bitmap area of the RAM 22 is DMA-transferred again to the DECU 41 via the system bus SB (symbol T15). The DECU 41 DMA-transfers the recording data to the head controlling unit 33 via a third dedicated bus IB3 (symbol T16), then stores it in a register in the head controlling unit 33. The

head controlling unit 33 DMA-transfers the recording data stored in the register to the recording head 62 (symbol T17).

[0106] Fig. 12 is a block diagram showing the internal configurations of the DECU 41 and the receiving buffer unit 42. Fig. 13 shows the configuration of a header analyzing block of the receiving buffer unit 42. And, the DECU 41 and the receiving buffer unit 42 configured in the ASIC 4 will be described in further detail.

[0107] The receiving buffer unit 42 has an IF memory 425 in which the compressed recording data is stored, a data transfer controlling block 424 as a "data transfer controlling means" for storing the compressed recording data in the IF memory 425, a command storing register 426 in which the command is stored, a header analyzing block 423 as a "header analyzing means" for analyzing the header of the record controlling data, a change controlling block 422 as a "command separating means" for separating the command from the record controlling data based on the analysis result of the header analyzing block 423, storing the command in the command storing register 426, transferring the record controlling data after command separation to the data transfer controlling block 424 and storing it in the IF memory 425 and a data separating block 427 as a "data separating means" for separating the record controlling data stored in the IF memory 425 into the remote command and the compressed recording data. The IF memory 425 is a FIFO (First In First Out) memory, which is well-known. In addition, the receiving buffer unit 42 has an I-DMA controller 421 for controlling DMA transfer performed via the first dedicated bus IB1 with the interface unit 27.

[0108] When the transfer of the record controlling data between the information processing apparatus 200 and the inkjet type recording apparatus 50 is started, the record controlling data received by the interface unit 27 is DMA-transferred to the receiving buffer unit 42 via the first dedicated bus IB1. The

record controlling data DMA-transferred to the received buffer unit 42 is transferred to the change controlling block 422, which changes the data transfer route of the record controlling data inside the receiving buffer unit 42. The change controlling block 422 is a block for transferring the record controlling data DMA-transferred from the interface unit 27 to one of the header analyzing block 423, the data transfer controlling block 424 and the command storing register 426, and this data transfer route is controlled by the header controlling block 423. At the data transfer start, the data transfer route of the change controlling block 422 is toward the header analyzing block 423, and first the header analysis is performed in the header analyzing block 423.

[0109] In regard to the data communication format according to the present invention, a header of 6 bytes is added to the record controlling data, and the header is stored in a 6 bytes register 431 to be analyzed. In regard to the configuration of the header, the first two bytes are a channel, the next two bytes are a length and the next two bytes are the data, which is used for negotiation of data communication in order that the interface unit 27 can confirm and determine communication conditions or a communication protocol about hardware with the information processing apparatus 200. The channel indicates whether the data following the header is the command or the compressed recording data, and the data from 00H or 02H is the command and the data from 40H is the remote command and the compressed recording data. The upper byte indicates receiving while the lower byte indicates sending. The length is the amount (bytes) of the data included in the header. The command is such controlling command as feeding control, transfer control and discharge control of the recording papers and drive control of the carriage 61 in order to perform recording control in regard to the inkjet type recording apparatus 50.

[0110] The header analyzing block 423, in case the data following the header is the command after the channel analyzing

block 432 analyzes the header of first two bytes, changes the data transfer route of the change controlling block 422 to the command storing register 426 and stores the data of some bytes, which have been analyzed by the length analyzing block 433, into the command storing register 426. In addition, in case the data following the header is the remote command and the compressed recording data after the channel analyzing block 432 analyzes the header of first two bytes, the header analyzing block 423 changes the data transfer route of the change controlling block 422 to the data transfer controlling block 424, informs the data transfer controlling block 424 of the number of bytes, which have been analyzed, and transfers the data of those bytes into the data transfer controlling block 424. For example, when the data shown in Fig. 13 is stored in the header, the channel is 40H while the length is FFH, and thus the remote command and the compressed recording data are 255 bytes including the header, that is, the remote command and the compressed recording data following the header are 249 bytes, and therefore the data of 249 bytes following the header is transferred to the data transfer controlling block 424.

[0111] In regard to the command stored in the command storing register 426, the MPU 24 accesses it via the system bus SB to perform command analysis. The remote command and the compressed recording data transferred to the data transfer controlling block 424 are stored in the IF memory 425. The remote command and the compressed recording data stored in the IF memory 425 are DMA-transferred to the DECU 41 via the second dedicated bus IB2 responding to the data transfer request from the DECU 41. At this time, if the data observed by the MPU 24 is the remote command in regard to the data separating block 427, the MPU 24 performs command analysis on the remote command not to transfer it to the DECU 41, and only the compressed recording data is DMA-transferred to the DECU 41. Further, if the data communication format between the information processing apparatus 200 and the interface unit 27 is the data

communication format without a header, the header analysis is not performed in the header analyzing block 423, and after the data received by the interface unit 27 is stored in the IF memory 425 as it is, the remote command is separated from the data, then the MPU 24 performs remote command analysis on it.

[0112] The DECU 41 has a first I-DMA controller 411, a second I-DMA controller 415 and an S-DMA controller 413 as the "DMA-transferring means". The first I-DMA controller 411 for controlling DMA transfer through the second dedicated bus IB2 DMA-transfers the compressed recording data stored in the IF memory 425 of the receiving buffer unit 42 to a development processing controller 412 one word each. The development processing controller 412 includes the decode circuit 28 and the line buffer 281. The compressed recording data DMA-transferred from the IF memory 425 of the receiving buffer unit 42 one word each is hardware-developed by the decode circuit 28 one word each, and the developed recording data is stored and accumulated in the line buffer 281.

[0113] The S-DMA controller 413 controls DMA transfer through the system bus SB. In addition, a memory controller 414 controls retrieving and writing data in regard to the RAM 22 coupled to the system bus SB. And, when developed recording data of predetermined bytes has been accumulated in the line buffer 281, it is DMA-transferred to the RAM 22 through the system bus SB via the memory controller 414 by the S-DMA controller 413. The recording data developed and DMA-transferred to the RAM 22 is stored in the predetermined bitmap area of the RAM 22. The second I-DMA controller 415 controls DMA transfer through the third dedicated bus IB3. The developed recording data stored in the bitmap area of the RAM 22 is DMA-transferred to the head controlling unit 33 through the system bus SB and the third dedicated bus IB3 via the memory controller 414 by the second I-DMA controller 415, then stored in a register in the head controlling unit 33 and then

DMA-transferred to the recording head 62.

[0114] In addition, the DMA transfer from the line buffer 281 to the RAM 22 is transferred in burst by the S-DMA controller 413, and the DMA transfer from the RAM 22 to the recording head 62 is transferred in burst by the second I-DMA controller 415. As described above, the burst transfer is such data transfer method as, when the continuous data is transferred, the data is transferred occupying a bus until all data of a predetermined data block is completely transferred by omitting a part of a sequence such as an address designation. The S-DMA controller 413, when the developed recording data of predetermined bytes has been accumulated in the line buffer 281, transfers in burst the developed recording data of predetermined bytes one word each, occupying the system bus SB until the data of predetermined bytes is completely DMA-transferred to the RAM 22. The second I-DMA controller 415 transfers in burst the developed recording data stored in the bitmap area of the RAM 22 one word per a data block of predetermined bytes, occupying the system bus SB until all of one data block has been completely DMA-transferred to the recording head 62. Further, the development process of compressed recording data after it is transferred to the DECU 41 and the flow of the developed recording data will not be described because they are similar to those of the first embodiment described above.

[0115] In this way, the header analysis process of the record controlling data on which the conventional program performs software process and the processes storing the command into the command storing register 426 and storing the compressed recording data into the IF memory 425 by separating the command from the record controlling data based on the header analysis result are performed in the receiving buffer unit 42. And, the record controlling data received by the interface unit 27 via the first dedicated bus IB1 is transferred to the receiving buffer unit 42, and the record controlling data stored in the IF memory 425 of

the receiving buffer unit 42 is separated into the remote command and the compressed recording data. And, only the compressed recording data is transferred to the DECU 41, and the recording data developed by the decode circuit 28 is transferred from the RAM 22 to the head controlling unit 33 via the third dedicate bus IB3 after stored in the RAM 22 in advance. The command and the remote command are analyzed in the MPU 24. Owing to this, since the data transfer load of the system bus and the processing load of the MPU 24 can be significantly reduced, data transfer can be performed while the dependence on the MPU 24 is considerably low, and thus the data transfer processes between the interface unit 27 and the receiving buffer unit 42, between the receiving buffer unit 27 and the DECU 41 and between the DECU 41 and the recording head 62 can be performed at higher speed.

[0116] Further, as a third embodiment of the inkjet type recording apparatus 50 relating to the present invention, added to the second embodiment described above, header analysis is performed not by the receiving buffer unit 42 buy by an interface unit 27.

[0117] Fig. 14 is a block diagram showing the third embodiment of the data transferring apparatus 10.

[0118] The interface unit 27 has an I/F block 271 as a means for sending and receiving data to and from the information processing apparatus 200 taking the information processing apparatus 200 as a host apparatus in a predetermined data transfer sequence, a command storing register 426 in which the command is stored, a header analyzing block 423 as a "header analyzing means" for analyzing the header of the record controlling data, a change controlling block 422 as a "command separating means" for separating the command from the record controlling data based on the analysis result of the header analyzing block 423, storing the command in the command storing register 426, transferring the record controlling data after command separation to the data

transfer controlling block 424 and storing it in the IF memory 425 and a data transfer controlling block 424 as a "data transfer controlling means" for storing the compressed recording data in the IF memory 425. In addition, the receiving unit 42 has an I-DMA controller 421 for controlling DMA transfer performed via the first dedicated bus IB1 with the interface unit 27, an IF memory 425 in which the compressed recording data is stored and a data separating block 427 as a "data separating means" for separating the record controlling data stored in the IF memory 425 into the remote command and the compressed recording data.

[0119] When the transfer of the record controlling data between the information processing apparatus 200 and the inkjet type recording apparatus 50 is started, the record controlling data received by the I/F block 271 is DMA-transferred to the change controlling block 422, which changes the data transfer route of the record controlling data inside the interface unit 27. The change controlling block 422 is a block for transferring the record controlling data received by the I/F block 271 to one of the header analyzing block 423, the data transfer controlling block 424 and the command storing register 426, and this data transfer route is controlled by the header controlling block 423. At the data transfer start, the data transfer route of the change controlling block 422 is toward the header analyzing block 423, and first the header analysis is performed in the header analyzing block 423.

[0120] In regard to the data communication format according to the present invention, like the second embodiment described above, a header of 6 bytes is added to the record controlling data, and the header is stored in a 6 bytes register 431 of the header analyzing block 423 to be analyzed. In regard to the configuration of the header and the configuration of the header analyzing block, they will not be described because they are similar to those of the second embodiment.

[0121] In regard to the command stored in the command storing

register 426, the MPU 24 accesses it via the system bus SB to perform command analysis. The remote command and the compressed recording data transferred to the data transfer controlling block 424 are DMA-transferred to the receiving buffer unit 42 by the I-DMA controller 421 of the receiving buffer unit 42 via the first dedicated bus IB1 and are stored in the IF memory 425. The remote command and the compressed recording data stored in the IF memory 425 are DMA-transferred to the DECU 41 via the second dedicated bus IB2 responding to the data transfer request from the DECU 41. At this time, if the data observed by the MPU 24 is the remote command in regard to the data separating block 427, the MPU 24 performs command analysis on the remote command not to transfer it to the DECU 41, and only the compressed recording data is DMA-transferred to the DECU 41. Further, if the data communication format between the information processing apparatus 200 and the interface unit 27 is the data communication format without a header, the header analysis in not performed in the header analyzing block 423, and after the data received by the interface unit 27 is stored in the IF memory 425 as it is, the remote command is separated from the data, and then the MPU 24 performs remote command analysis on it.

[0122] Hereinafter, the configuration of the DECU 41 and the flow of data will not be described because they are similar to those of the second embodiment described above. In this way, the header analysis of the record controlling data may be performed by the interface unit 27, and, like the second embodiment described above, since the data transfer load of the system bus and the processing load of the MPU 24 can be significantly reduced, data transfer can be performed while the dependence on the MPU 24 is considerably low, and thus the data transfer processes between the interface unit 27 and the receiving buffer unit 42, between the receiving buffer unit 27 and the DECU 41 and between the DECU 41 and the recording head 62 can be performed at higher speed.

[0123] Although the invention has been described in its preferred form with a certain degree of particularity, obviously many changes and variations are possible therein. It is therefore to be understood that the present invention may be practiced than as specifically described herein without departing from scope and the sprit thereof.